

THE CLAIMS

1-35 (Canceled)

36. (Original) A transistor comprising:

a source region, a drain region, a channel region between the source and drain regions, and a gate separated from the channel region by an insulator, the gate formed of a silicon carbide compound $\text{Si}_{1-x}\text{C}_x$, wherein x is greater than 0.5 to establish a desired value of a barrier energy between the gate and the insulator.

37. (Original) A transistor comprising:

a source region, a drain region, a channel region between the source and drain regions, and a gate separated from the channel region by an insulator, the gate formed of a silicon carbide compound $\text{Si}_{1-x}\text{C}_x$, wherein x is selected at a predetermined value approximately between 0.5 and 1.0 to establish a desired value of a barrier energy between the gate and the insulator.

38. (Original) The transistor of claim 36, wherein the value of the barrier energy is approximately between 0 eV and 2.8 eV.

39. (Original) The transistor of claim 36, wherein the insulator is formed of silicon dioxide.

40-58 (Canceled)

59. (Original) A transistor comprising:

a source region formed in a substrate;
a drain region formed in the substrate;
a channel region in the substrate between the source region and the drain region; and
a gate separated from the channel region by an insulator, the gate comprising a silicon carbide compound $\text{Si}_{1-x}\text{C}_x$, wherein x is selected to be between 0.5 and 1.0.

60. (Original) The transistor of claim 59 wherein:
- the substrate comprises a p-type silicon substrate;
 - the source region comprises an n+-type source region formed in the substrate;
 - the drain region comprises an n+-type drain region formed in the substrate; and
 - the insulator comprises a layer of silicon dioxide.
61. (Original) The transistor of claim 59 wherein the gate comprises a material selected from the group consisting of a monocrystalline silicon carbide compound, a polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.
62. (Original) A transistor comprising:
- a source region formed in a substrate;
 - a drain region formed in the substrate;
 - a channel region in the substrate between the source region and the drain region; and
 - a gate separated from the channel region by an insulator, the gate comprising a silicon carbide compound $\text{Si}_{1-x}\text{C}_x$, wherein x is selected to be between 0.1 and 0.5.
63. (Original) The transistor of claim 62 wherein:
- the substrate comprises a p-type silicon substrate;
 - the source region comprises an n+-type source region formed in the substrate;
 - the drain region comprises an n+-type drain region formed in the substrate; and
 - the insulator comprises a layer of silicon dioxide.
64. (Original) The transistor of claim 62 wherein the gate comprises a material selected from the group consisting of a monocrystalline silicon carbide compound, a polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.

65. (Original) A transistor comprising:
- a source region formed in a substrate;
 - a drain region formed in the substrate;
 - a channel region in the substrate between the source region and the drain region; and
 - a gate separated from the channel region by an insulator, the gate comprising a silicon carbide compound $\text{Si}_{1-x}\text{C}_x$, wherein x is selected to be less than 0.5.
66. (Original) The transistor of claim 65 wherein:
- the substrate comprises a p-type silicon substrate;
 - the source region comprises an n+-type source region formed in the substrate;
 - the drain region comprises an n+-type drain region formed in the substrate; and
 - the insulator comprises a layer of silicon dioxide.
67. (Original) The transistor of claim 65 wherein the gate comprises a material selected from the group consisting of a monocrystalline silicon carbide compound, a polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.
- 68-70 (Canceled)
71. (Original) A floating gate transistor comprising:
- a source region formed in a substrate;
 - a drain region formed in the substrate;
 - a channel region in the substrate between the source region and the drain region;
 - a floating gate separated from the channel region by an insulator, the floating gate comprising a silicon carbide compound $\text{Si}_{1-x}\text{C}_x$, wherein x is selected to be between 0.5 and 1.0;
- and
- a control gate separated from the floating gate by an intergate dielectric.

72. (Original) The floating gate transistor of claim 71 wherein:
- the substrate comprises a p-type silicon substrate;
 - the source region comprises an n+-type source region formed in the substrate;
 - the drain region comprises an n+-type drain region formed in the substrate;
 - the insulator comprises silicon dioxide; and
 - the intergate dielectric comprises silicon dioxide.
73. (Original) The floating gate transistor of claim 71 wherein the floating gate comprises a material selected from the group consisting of a monocrystalline silicon carbide compound, a polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.
74. (Original) A floating gate transistor comprising:
- a source region formed in a substrate;
 - a drain region formed in the substrate;
 - a channel region in the substrate between the source region and the drain region;
 - a floating gate separated from the channel region by an insulator, the floating gate comprising a silicon carbide compound $\text{Si}_{1-x}\text{C}_x$, wherein x is selected to be between 0.1 and 0.5;
- and
- a control gate separated from the floating gate by an intergate dielectric.
75. (Original) The floating gate transistor of claim 74 wherein:
- the substrate comprises a p-type silicon substrate;
 - the source region comprises an n+-type source region formed in the substrate;
 - the drain region comprises an n+-type drain region formed in the substrate;
 - the insulator comprises silicon dioxide; and
 - the intergate dielectric comprises silicon dioxide.

76. (Original) The floating gate transistor of claim 74 wherein the floating gate comprises a material selected from the group consisting of a monocrystalline silicon carbide compound, a polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.

77. (Original) A floating gate transistor comprising:

- a source region formed in a substrate;
- a drain region formed in the substrate;
- a channel region in the substrate between the source region and the drain region;
- a floating gate separated from the channel region by an insulator, the floating gate comprising a silicon carbide compound $\text{Si}_{1-x}\text{C}_x$, wherein x is selected to be less than 0.5;

and

- a control gate separated from the floating gate by an intergate dielectric.

78. (Original) The floating gate transistor of claim 77 wherein:

- the substrate comprises a p-type silicon substrate;
- the source region comprises an n+-type source region formed in the substrate;
- the drain region comprises an n+-type drain region formed in the substrate;
- the insulator comprises silicon dioxide; and
- the intergate dielectric comprises silicon dioxide.

79. (Original) The floating gate transistor of claim 77 wherein the floating gate comprises a material selected from the group consisting of a monocrystalline silicon carbide compound, a polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.

80. (Original) A floating gate transistor comprising:

- a source region formed in a substrate;
- a drain region formed in the substrate;
- a channel region in the substrate between the source region and the drain region;

a floating gate separated from the channel region by an insulator, the floating gate comprising a silicon carbide compound $\text{Si}_{1-x}\text{C}_x$, wherein x is selected to be between 0.5 and 0.75; and

a control gate separated from the floating gate by an intergate dielectric.

81. (Original) The floating gate transistor of claim 80 wherein:

the substrate comprises a p-type silicon substrate;

the source region comprises an n+-type source region formed in the substrate;

the drain region comprises an n+-type drain region formed in the substrate;

the insulator comprises silicon dioxide; and

the intergate dielectric comprises silicon dioxide.

82. (Original) The floating gate transistor of claim 80 wherein the floating gate comprises a material selected from the group consisting of a monocrystalline silicon carbide compound, a polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.

83. (Original) A floating gate transistor comprising:

a source region formed in a substrate;

a drain region formed in the substrate;

a channel region in the substrate between the source region and the drain region;

a floating gate separated from the channel region by an insulator, the floating gate comprising a silicon carbide compound $\text{Si}_{1-x}\text{C}_x$, wherein x is selected to be between 0.75 and 1.0; and

a control gate separated from the floating gate by an intergate dielectric.

84. (Original) The floating gate transistor of claim 83 wherein:

the substrate comprises a p-type silicon substrate;

the source region comprises an n+-type source region formed in the substrate;

the drain region comprises an n+-type drain region formed in the substrate;

the insulator comprises silicon dioxide; and
the intergate dielectric comprises silicon dioxide.

85. (Original) The floating gate transistor of claim 83 wherein the floating gate comprises a material selected from the group consisting of a monocrystalline silicon carbide compound, a polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.

86-97 (Canceled)

98. (Original) The transistor of claim 36, wherein the gate is an electrically isolated floating gate and further comprising a control gate, separated from the floating gate by an intergate dielectric comprising silicon dioxide.

99. (Original) The transistor of claim 37 wherein:
the insulator comprises silicon dioxide; and
the gate comprises a material selected from the group consisting of a monocrystalline silicon carbide compound, a polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.

100 (Canceled)